Shashwat Shrivastava

Resume

EPFL
+41 762637453
talk2shashwat@gmail.com

My background spans hardware accelerator design and EDA/compiler development, with experience in RTL development using Verilog, pipelined and parallel compute architectures, on-chip memory systems, and runtime-configurable hardware. I also bring strong C++ and algorithm development experience, including performance optimization and working with AMD's Vivado C++ codebase.

Education

2021–2026 **Ph.D. in Computer and Communication Sciences**, *EPFL*
Thesis: From Monolithic to Multi-Stage Routing for FPGAs
Research focus: FPGA compilation acceleration, with applications to emulation and prototyping; routing algorithms and compiler–architecture co-design
Advisors: Dr. Mirjana Stojilović and Prof. Babak Falsafi
Relevant experience: EDA tool development, FPGA interconnect architecture, code-level and algorithmic runtime optimization, graph and routing algorithms, data structures, C++, Python, diagnostic frameworks, and bottleneck identification and analysis

2016–2021 **B.Tech. and M.S. by Research in Electronics and Communication**, *IIIT-Hyderabad*
Research focus: FPGA accelerator design, parallel compute architectures, and streaming memory systems
Advisor: Prof. Suresh Purini
Relevant experience: Pipelined datapaths, data-level parallelism, configurable architectures, on-chip buffering, data reuse, prefetching, compute–communication overlap, BSV, Verilog, AXI4, TensorFlow, OpenCL, Vivado, Vitis, Xilinx Virtex-7, and AWS F1 FPGAs

Work Experience

Jun–Dec 2023 **Research Intern**, *AMD*, Longmont, Colorado, USA
- Integrated our routing approach into the Vivado C++ codebase
- Evaluated its runtime impact for AMD FPGAs targeting emulation and prototyping
- Explored FPGA interconnect modifications to reduce routing complexity and runtime

Jan–Jul 2021 **Research Intern**, *Intel Labs*, Bangalore, India
- Implemented memory subsystems and data-preparation software for 3D segmentation
- Contributed to Verilog RTL, C++ host software, and firmware

May–Aug 2019 **Student Developer**, *Google Summer of Code*, Hyderabad, India
- Developed dynamic and interactive simulation capabilities for a robotics simulator

May–Jul 2018 **Research Intern**, *Bluespec Inc.*, Mysore, India
- Explored the hardware design space for dense matrix multiplication

Technical Skills

Programming C, C++, Python, MATLAB, Bash, OpenCL

HDLs	Verilog, SystemVerilog, Bluespec SystemVerilog (BSV)
HW Design	RTL design, FPGA architecture, AXI4 (full, lite, stream)
EDA tools	Verilog-to-Routing (VTR), Yosys, OpenROAD, Vivado, Vitis, HLS
Platforms	AMD Virtex-7, AWS F1, Xillybus, RunAI

Publications

FCCM'26 **PathSteiner: Improving PathFinder with Quasi-Optimal Steiner-Tree Initialization**

Shashwat Shrivastava, Luka Kurešević, Alex Poupakis, Chirag Ravishankar, Dinesh Gaitonde, Stefan Nikolić, Mirjana Stojilović

- Implemented an ASIC-style multi-stage router in the VTR C++ codebase
- Optimized coarse-path following to reduce data movement and access time
- Integrated FLUTE, an RSMT algorithm, into VTR and adapted it for large FPGAs
- Achieved up to 8× routing speedup on the most congested benchmark

FCCM'25 **Guaranteed Yet Hard to Find: Uncovering FPGA Routing Convergence Paradox**

Best Paper

Shashwat Shrivastava, Stefan Nikolić, Sun Tanaka, Chirag Ravishankar, Dinesh Gaitonde, Mirjana Stojilović

- Built a routing-failure diagnosis framework using Python, VTR C++, and hMETIS
- Uncovered a core **inefficiency in the 30-year-old SOTA** PathFinder routing algorithm

ICCAD'23 **IIBLAST: Speeding Up Commercial FPGA Routing by Decoupling and Mitigating the Intra-CLB Bottleneck**

Shashwat Shrivastava, Stefan Nikolić, Chirag Ravishankar, Dinesh Gaitonde, M. Stojilović

- Identified a core routing-runtime bottleneck in commercial FPGA architectures
- Co-designed the routing algorithm and architecture to alleviate this bottleneck

HaSS'23 **Instruction-Level Power Leakage Evaluation of Soft-Core CPUs on FPGAs**

Ognjen Glamočanin, **Shashwat Shrivastava**, Jinwei Yao, Nour Ardo, Mathias Payer, Mirjana Stojilović

ACM TACO'22 **An FPGA Overlay for CNN Inference with Fine-grained Flexible Parallelism**

Ziaul Choudhury, **Shashwat Shrivastava**, Lavanya Ramapantulu, Suresh Purini

- Developed a **runtime-configurable** CNN accelerator programmable using TensorFlow
- Implemented **pipelined PEs** with configurable data distribution and **DSP multipliers**
- Optimized buffering and weight **prefetching** for data reuse and compute–memory overlap

FPL'21 **FPGA Accelerator for Stereo Vision using Semi-Global Matching through Dependency Relaxation**

Shashwat Shrivastava, Ziaul Choudhury, Shashwat Khandelwal, Suresh Purini

- Implemented a **stall-free, pipelined accelerator** exploiting data-level parallelism
- Designed a **streaming memory architecture** to overlap compute and data transfer
- Achieved 322 frames/s at 100 MHz for 1280×960 images on a Virtex-7 FPGA

FPL'21 **Accelerating Local Laplacian Filters on FPGAs**

Shashwat Khandelwal, Ziaul Choudhury, **Shashwat Shrivastava**, and Suresh Purini

Honours and Awards

- Best Paper Award at FCCM'25 (one of the leading FPGA conferences)
- EPFL EDIC Fellowship (competitive fellowship for incoming Ph.D. students)
- Dean's List, IIIT-H, 2017–19 (awarded to students in the top 5%)