Shashwat Shrivastava

Resume

EPFL
+41 762637453
talk2shashwat@gmail.com

Education

2021-2026 **Ph.D. in Computer and Communication Sciences**, *EPFL*
Thesis: From Monolithic to Multi-Stage Routing for FPGAs
Research focus: FPGA compilation, with applications to emulation and prototyping; routing algorithms and compiler–architecture co-design
Advisors: Dr. Mirjana Stojilović and Prof. Babak Falsafi
Relevant experience: FPGA architecture modeling, VTR, C/C++, Python, graph and routing algorithms, hMETIS, ILP-based architecture optimization, and performance analysis and optimization

2016-2021 **B.Tech. and M.S. by Research in Electronics and Communication**, *IIIT-Hyderabad*
Research focus: FPGA acceleration of stereo vision, local Laplacian filtering, and CNN workloads using Bluespec SystemVerilog
Advisor: Prof. Suresh Purini
Relevant experience: Bluespec SystemVerilog, Verilog, OpenCL, Vivado, Vitis; Xilinx Virtex-7 and AWS F1 FPGAs

Work Experience

Jun–Dec 2023 **Research Intern**, *AMD*, Longmont, Colorado, USA
- Integrated our routing approach into the Vivado C++ codebase
- Evaluated its runtime impact for AMD FPGAs targeting emulation and prototyping
- Explored FPGA architecture modifications to reduce routing complexity and runtime

Jan–Jul 2021 **Research Intern**, *Intel Labs*, Bangalore, India
- Hardware–software co-design for accelerating 3D image segmentation
- Contributed to Verilog RTL, C++ host software, and firmware

May–Aug 2019 **Student Developer**, *Google Summer of Code*, Hyderabad, India
- Developed dynamic and interactive simulation capabilities for a robotics simulator

May–Jul 2018 **Research Intern**, *Bluespec Inc.*, Mysore, India
- Explored the hardware design space for dense matrix multiplication

Technical Skills

Programming C, C++, Python, MATLAB, Bash, OpenCL
HDLs Verilog, SystemVerilog, Bluespec SystemVerilog
HW Design RTL design, FPGA architecture
EDA tools Verilog-to-Routing (VTR), Yosys, OpenROAD, Vivado, Vitis, HLS
Platforms AMD Virtex-7, AWS F1, Xillybus, RunAI

Publications

FCCM'26 **PathSteiner: Improving PathFinder with Quasi-Optimal Steiner-Tree Initialization**
Shashwat Shrivastava, Luka Kurešević, Alex Poupakis, Chirag Ravishankar, Dinesh Gaitonde, Stefan Nikolić, Mirjana Stojilović
- Implemented a new routing algorithm in the VTR C++ codebase
- Integrated FLUTE, an RSMT algorithm, into VTR and adapted it for large FPGAs
- Developed an algorithm for diagonal decomposition of FLUTE trees on a 2D grid
- Achieved up to 8× routing-runtime improvement on the most congested benchmark

FCCM'25 **Guaranteed Yet Hard to Find: Uncovering FPGA Routing Convergence Paradox**
Best Paper
Shashwat Shrivastava, Stefan Nikolić, Sun Tanaka, Chirag Ravishankar, Dinesh Gaitonde, Mirjana Stojilović
- Built a routing-failure diagnosis framework using Python, VTR C++, and hMETIS
- Uncovered a core inefficiency in the 30-year-old SOTA PathFinder routing algorithm

ICCAD'23 **IIBLAST: Speeding Up Commercial FPGA Routing by Decoupling and Mitigating the Intra-CLB Bottleneck**
Shashwat Shrivastava, Stefan Nikolić, Chirag Ravishankar, Dinesh Gaitonde, Mirjana
- Built a VTR-compatible framework for arbitrary FPGA routing-graph generation
- Implemented our new routing algorithm using Python and C++ in VTR

HaSS'23 **Instruction-Level Power Leakage Evaluation of Soft-Core CPUs on FPGAs**
Ognjen Glamočanin, **Shashwat Shrivastava**, Jinwei Yao, Nour Ardo, Mathias Payer, Mirjana Stojilović

ACM TACO'22 **An FPGA Overlay for CNN Inference with Fine-grained Flexible Parallelism**
Ziaul Choudhury, **Shashwat Shrivastava**, Lavanya Ramapantulu, Suresh Purini

FPL'21 **FPGA Accelerator for Stereo Vision using Semi-Global Matching through Dependency Relaxation**
Shashwat Shrivastava, Ziaul Choudhury, Shashwat Khandelwal, Suresh Purini
- Designed and implemented the accelerator in Bluespec SystemVerilog
- Developed a host-side software interface for data transfer to and from the FPGA

FPL'21 **Accelerating Local Laplacian Filters on FPGAs**
Shashwat Khandelwal, Ziaul Choudhury, **Shashwat Shrivastava**, and Suresh Purini

Honours and Awards

- Best Paper Award at FCCM'25 (one of the leading FPGA conferences)
- EPFL EDIC Fellowship (competitive fellowship for incoming Ph.D. students)
- Dean's List, IIIT-H, 2017–19 (awarded to students in the top 5%)

Talks

FCCM'26 PathSteiner: Improving PathFinder with Quasi-Optimal Steiner-Tree Initialization
FCCM'25 Uncovering FPGA Routing Convergence Paradox
EPFL'24 Accelerating ASIC Emulation and Prototyping
ICCAD'23 IIBLAST: Speeding Up Commercial FPGA Routing
HiPEAC'23 An FPGA Overlay for CNN Inference
FPL'21 FPGA Accelerator for Stereo Vision